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[5559]-202

S.E. (I.T.) (Third Semester) EXAMINATION, 2019
COMPUTER ORGANISATION AND ARCHITECTURE
(2015 PATTERN)

Time : 2 Hours

Maximum Marks : 50

N.B. :— (i) Answer four questions.

(ii) Neat diagrams must be drawn wherever necessary.

(iii) Figures to the right side indicate full marks.

(iv) Assume suitable data if necessary.

1. (a) Multiply -7 and 3 using Booths Algorithm. [6]

(b) Describe the computer performance parameters such as CPU time, CPI, MIPS, MFLOPS, Amdahl's law and clock rate. [6]

Or

2. (a) Explain any three addressing modes with suitable example. [6]

(b) Differentiate between RISC and CISC Architecture. [6]

3. (a) Draw and explain single bus processor organisation. [6]

(b) What is Micro-instruction ? Explain micro-programmed control unit with the help of suitable diagram. [6]

Or

4. (a) How virtual memory is managed using paging and TLB ? [6]

(b) List and explain cache replacement policy. [6]

P.T.O.

5. (a) Explain basic performance issue of pipelining. [6]
(b) Explain data hazards and control hazards. [7]

Or

6. (a) Write short note on superscalar processor. [6]
(b) Explain five stage pipeline for MIPS architecture with diagram. [7]

7. (a) With the help of suitable diagram explain Flynn's Taxonomy for multiple processor organisation. [7]
(b) What is clustering ? Explain cluster architecture. [6]

Or

8. (a) What is Multicore Organisation ? Explain hardware and software issues involved in multi core organisation. [7]
(b) Explain loosely coupled and closely coupled microprocessor system. [6]